[0063] It is also understood that the examples and embodiments described herein are for illustrative purposes only and that various modifications or changes in light thereof will be suggested to persons skilled in the art and are to be included within the spirit and purview of this application and scope of the appended claims.

What is claimed is:

1. A method for fabricating an electronic device, the method comprising:

providing a III-nitride substrate;

forming a III-nitride epitaxial layer coupled to the III-nitride substrate, wherein the III-nitride epitaxial layer has an upper surface and a thickness;

removing a predetermined portion of the III-nitride epitaxial layer to form one or more recessed regions extending from the upper surface to a predetermined depth into the III-nitride epitaxial layer;

regrowing a III-nitride epitaxial material in the one or more recessed regions, wherein the III-nitride epitaxial material has an upper regrowth surface substantially coplanar with the upper surface of the III-nitride epitaxial layer.

2. The method of claim **1** further comprising

forming a first electrical contact to a contact region of the upper surface of the III-nitride epitaxial layer; and

forming a second electrical contact to a contact region of the upper regrowth surface.

3. The method of claim **1** wherein the III-nitride substrate comprises an n-type GaN substrate.

4. The method of claim **1** wherein the III-nitride layer comprises an n-type GaN epitaxial layer.

5. The method of claim **1** wherein the III-nitride epitaxial material comprises a p-type GaN epitaxial material.

6. The method of claim **1** wherein the III-nitride layer comprises a plurality of sub-layers including a drift sub-layer, a channel sub-layer, and a source sub-layer.

7. The method of claim **1** wherein the predetermined depth is less than the thickness.

8. A vertical JFET comprising:

a III-nitride substrate;

a III-nitride epitaxial layer of a first conductivity type coupled to the III-nitride substrate, wherein the first III-nitride epitaxial layer has a first dopant concentration;

a III-nitride epitaxial structure coupled to the first III-nitride epitaxial layer, wherein the III-nitride epitaxial structure comprises:

a set of channels of the first conductivity type and having a second dopant concentration;

a set of sources of the first conductivity type, having a third dopant concentration greater than the first dopant concentration, and each characterized by a contact surface;

a set of regrown gates interspersed between the set of channels, wherein an upper surface of the set of regrown gates is substantially coplanar with the contact surfaces of the set of sources.

9. The vertical JFET of claim **8** further comprising:

a set of source contacts, each being electrically coupled to the set of sources; and

a set of gate contacts, each being electrically coupled to the set of regrown gates.

10. The vertical JFET of claim **8** further comprising a drain contact electrically coupled to the III-nitride substrate.

11. The vertical JFET of claim **8** wherein the first conductivity type is n type and the set of regrown gates are p type.

12. The vertical JFET of claim **8** wherein at least one of the first dopant concentration, the second dopant concentration, or the third dopant concentration is non-uniform.

13. The vertical JFET of claim **8** wherein a thickness of the III-nitride epitaxial layer is between 1 μm and 100 μm.

14. The vertical JFET of claim **8** wherein the set of channels are disposed between gates of the set of regrown gates such that current flow during operation of the vertical JFET is along a direction orthogonal to the upper surface of the set of regrown gates.

15. The vertical JFET of claim **8** wherein the III-nitride substrate comprises an n-type substrate.

16. The vertical JFET of claim **8** wherein the III-nitride epitaxial layer comprises an n-type GaN epitaxial layer having a dopant concentration less than or equal to a dopant concentration of the III-nitride substrate and a thickness greater than 1 μm.

17. The vertical JFET of claim **8** wherein a width of the set of channels measured along a direction orthogonal to a thickness of the III-nitride epitaxial layer is less than 5 μm.

18. The vertical JFET of claim **8** wherein the set of gates comprise a p-type III-nitride material.

19. The vertical JFET of claim **8** wherein the set of gates are further electrically coupled to the drift region.

20. A method of fabricating a vertical JFET, the method comprising:

providing a III-nitride substrate;

forming a first III-nitride epitaxial layer of a first conductivity type coupled to the III-nitride substrate, wherein the first III-nitride epitaxial layer has a first thickness;

forming one or more additional III-nitride epitaxial layers coupled to the first III-nitride epitaxial layer;

removing a portion of the one or more additional III-nitride epitaxial layers to form a set of recesses extending a predetermined distance into the one or more additional III-nitride epitaxial layers, wherein the set of recesses are disposed between remaining portions of the one or more additional III-nitride epitaxial layers;

regrowing an epitaxial material in the set of recesses, wherein the epitaxial material has a thickness substantially equal to the predetermined distance;

forming a drain contact electrically coupled to the III-nitride substrate;

forming a set of source contacts electrically coupled to the remaining portions of the one or more additional III-nitride epitaxial layers; and

forming a set of gate contacts electrically coupled to the epitaxial material.

21. The method of claim **20** wherein the epitaxial material has a thickness within 10% of the predetermined distance.

22. The method of claim **20** wherein the set of source contacts are substantially coplanar with the set of gate contacts.

23. The method of claim **20** wherein the one or more additional epitaxial layers comprise a second III-nitride epitaxial layer coupled to the first III-nitride epitaxial layer and a third III-nitride epitaxial layer coupled to the second III-nitride epitaxial layer, wherein the epitaxial material extends through the third III-nitride epitaxial material into a portion of the third III-nitride epitaxial layer.

24. The method of claim **20** wherein the epitaxial material comprises gate regions of the vertical JFET.